HEART 2014 Design Contest

#	Authors	Institution	Team	Code	Device	Strategy, tool etc.	Title	Ctegory	HDL	HLS	CPU	GPU	Other
1	Lin Meng, Daichi Kinekawa, Haruaki Ishikawa, Katsuhiro Yamazaki and Shogo Masuda	Ritsumeikan Univ.	Mt.Cape	YA	DE2-115	Alpha-Beta / Impulse C	Development of a Blokus-Duo Algorithm with a FPGA Board	Regular FPGA		o			
2	Masashi Ohno, Kazuya Ohtsu and Tomonori Izumi	Ritsumeikan Univ.	BLUE STORM	RB	Nexys4 XC7A100T	Minmax-based search / Impulse C	BLUE STORM : BLokus Unified Engine of Search and Test Operation by RitsuMei	Regular FPGA		o			
3	Yuta Nakatani, Yuichiro Tanaka, Hiroshi Nakatsuka and Atsushi Takahashi	Tokyo Institute of Tech.	TNT	TN	Nexys4 XC7A100T	Min-max based search / PlanAhead	Blokus Duo Attacker by Parallel Processing	Regular FPGA	o				
4	Retsu Moriwaki, Takumi Fujimori, Takashi Yoza, Masato Seo, Kouta Akagi, Yuki Torigai and Minoru Watanabe	Shizuoka Univ.	Blokus Duo Solver I	BD	Arriall GX	Alpha-Beta	FPGA Blokus Duo Solver on an Arria II GX FPGA	Regular FPGA	o				
5	Retsu Moriwaki, Takumi Fujimori, Takashi Yoza, Masato Seo, Kouta Akagi, Yuki Torigai and Minoru Watanabe	Shizuoka Univ.	Blokus Duo Solver II	BE	StartixV 5SGXA7	Extended version of #4	Blokus Duo Solver System including an Ultra Large FPGA	Unlimted	o		o		
6	Naru Sugimoto and Hideharu Amano	Keio Univ.	Cry-Wolf	HF	Nexys4 XC7A100T	Alpha-Beta / CWB	Blokus Duo Solver on FPGA Using Cyber Work Bench	Regular FPGA		o			
7	Kaoru Hamasaki, Koji Okina, Aiko Iwasaki, Jimpei Hamamura and Yuichiro Shibata	Nagasaki Univ.	Sakura-Duo	SD	DE2-115	Monte-Carlo tree search / stream	SAKURA-Duo: FPGA Implementation of Monte-Carlo Tree Search for Blokus-Duo	Regular FPGA	o				
9	Keisei Takayama, Kouki Itajima, Nobuya Watanabe and Akira Nagoya	Okayama Univ.	Harekus	OU	DE2-115	Alpha-Beta	Improvement of the Blokus Duo Implementation on FPGA using SFL	Regular FPGA	o				
10	Komei Nomura, Asuka Shinohara, Kazuo Teshima and Yasuhiro Takashima	Kitakyushu City Univ.	KRAB	KR	DE2-115	Zone concept: alpha-beta based	K.R.A.B. --Blokus-duo engine with High-level synthesis --	Regular FPGA		o			
11	Hirotaka Takayama and Yoshiki Yamaguchi	Univ. of Tsukuba	lila.cs	LI	Atlys XC6SLX45	Alpha-Beta	Blokus Duo Solver using evaluation of the exact domain	Regular FPGA	o				
12	Ken-Ichi Suzuki	Tohoku Institute of Tech.	Ponkotsu	TS	DE2-115	Monte-Carlo w/NIOS	A BlokusDuo Solver on FPGA containing AVR cores	Regular FPGA	o				
13	Takuji Mitsuishi, Naru Sugimoto and Hideharu Amano	Keio Univ.	Healthy Ninja	HN	GeForce GTX 780 Ti	Monte-Carlo	Blokus Duo Solver on GPU	Unlimted				o	
14	Masataka Ogawa, Yuki Ando, Shinya Honda and Yusuke Kato	Nagoya Univ.	TEAM ERTL	ER	DE2-115	Depth-first search / CWB	ERTL Blokus Solver II	Regular FPGA		o			
15	Kota Aoki, Masahito Oishi and Rie Soejima	Nagasaki Univ.	RS Blokus	RS		Alpha-Beta	FPGA implementation of α-β pruning for Blokus Duo	Regular FPGA	o				
16	Susumu Mashimo, Kansuke Fukuda, Masahiro Iida, Motoki Amagasaki, Morihiro Kuga and Toshinori Sueyoshi	Kumamoto Univ.	Kuma 2 Duo	KU	DE2-115	Alpha-Beta + Heuristic	Parallel Blokus Duo Game-playing Artifical-Intelligence on an FPGA	Regular FPGA	o				
18	Yuu Nakahara, Tatsuya Suzuki and Tomonori Izumi	Ritsumeikan Univ.	PulseR	PR	Nexys4 XC7A100T	Greedy simulation / Impulse C	PulseR - design of an artificial intelligence system with reconfigurable hardware and high-level synthesis	Regular FPGA		o			
19	Hiroki Nakahara and Koshiro Shiihara	Kagoshima Univ.	Suki!Suki!Skip!HKT48!!!	HK	VC707 XC7VX485T	Monte-Carlo Tree Search with Machine Learning	HKT48: a "H"ybrid system for blo"K"us-duo based on a "T"ransputer by "48" dedicated	Unlimited	o		o		
20	Tatsuya Komatsu, Yukimasa Okabayashi, Kohei Yamamoto, Toshiki Morioka, Yukio Mitsuyama	Kochi Univ. of Tech.	Y-Style	TK	DE2-115	HDL	FPGA-Based Blokus Duo Solver Design using High-Level Synthesis Environment	Regular FPGA	o				
21	Koshiro Shiihara and Hiroki Nakahara	Kagoshima Univ.	SATSUMA	SA	DE2-115	Monte-Carlo tree search	A blokus duo sovler using multi-core proseccor	Regular FPGA	o		o		
22	Tomoya Ueno, Kentaro Sano and Heewon Park	Tohoku Univ.	ABC	TP	DE2-115	Alpha-Beta w/NIOS	Blokus Duo Solver Using Soft-Core Processor and Hardware	Regular FPGA	o				
23	Keisuke Dohi and Xiongxin Zhao	Nagasaki Univ.	DohiBlokus	DB	DE2i-150 Cyclone IV EP4-150	Monte-Carlo tree search	Dohi Blokus: FPGA Implementation of Game AI for Blokus Duo	Regular FPGA	o				
24	Akira Kojima	Hiroshima City Univ.	Reconfigurable Application Diffusion Committee	RA	Nexys4 XC7A100T	Alpha-Beta	Blokus Duo FPGA Player using Hardware-Software Co-Design Approach	Regular FPGA	o				